Amendments to the Specification

Please amend the paragraph at page 10, line 27 to page 11, line 5, as follows:

Figure 2 illustrates a Ramsey Type-III interleaver 115 and a Ramsey Type-IV device 116 as the corresponding de-interleaver. As with devices 1, 2, devices 115, 116 respectively employ write commutators 117, 120; read commutators 119, 122; and row position pointers 124, 125 to perform interleaving and deinterleaving in respective memory arrays 118, 121. Similar to the number of rows, N, in FIG. 1, devices 115, 116 are designed to use I rows of memory cells. As with interleavers 1, 2, the operation of commutators 119, 120, and perhaps, row position pointers 124, 125, can employ a selected modulo-based technique. It is most desirable that each of the commutators 117 and 122, and 119 and 120, and the row position pointers, 124, 125, be synchronized.